PAAVAI ENGINEERING COLLEGE, NAMAKKAL – 637 018

(AUTONOMOUS)

M.E. APPLIED ELECTRONICS

REGULATIONS 2016

CURRICULUM

(CHOICE BASED CREDIT SYSTEM)

SEMESTER I

Course Code	Course Title	L	T	P	C
PMA16103	Applied Mathematics for Electronics Engineers	3	2	0	4
PAE16101	Advanced Digital Signal Processing	3	2	0	4
PAE16102	Advanced Digital Logic System Design	3	2	0	4
PAE16103	Advanced Microprocessor and Microcontroller	3	2	0	4
PAE16104	Multicore Architecture and Programming	3	2	0	4
PAE1615*	Elective I	3	0	0	3
PAE16105	Electronics System Design Laboratory I	0	0	4	2

SEMESTER II

Course Code	Course Title	L	T	P	C
PAE16201	Analysis and Design of Analog Integrated Circuits	3	2	0	4
PAE16202	ASIC and FPGA Design	3	2	0	4
PAE16203	Low Power VLSI Design	3	2	0	4
PAE1625*	Elective II	3	0	0	3
PAE1635*	Elective III	3	0	0	3
PAE1645*	Elective IV	3	0	0	3
PAE16207	Electronics System Design Laboratory II	0	0	4	2

LIST OF ELECTIVES

ELECTIVE I

Course Code	Course Title	L	T	P	C
PAE16151	Advanced Digital Image Processing	3	0	0	3
PAE16152	Wavelet Transforms and Applications	3	0	0	3
PAE16153	Physical Design of VLSI Circuits	3	0	0	3
PAE16154	Computer Architecture and Parallel Processing	3	0	0	3

ELECTIVE II

Course Code	Course Title	L	T	P	C
PAE16251	CAD for VLSI Circuits	3	0	0	3
PAE16252	Digital Control Engineering	3	0	0	3
PAE16253	VLSI Signal Processing	3	0	0	3
PAE16254	Sensors and Signal Conditioning	3	0	0	3

ELECTIVE III (OPEN ELECTIVE)

Course Code	Course Title	L	T	P	C
PAE16351	Mobile Networks	3	0	0	3
PAE16352	Soft Computing	3	0	0	3
PAE16353	High Performance Networks	3	0	0	3

ELECTIVE IV

Course Code	Course Title	L	T	P	C
PAE16451	VLSI Design Techniques	3	0	0	3
PAE16452	Fiber Optic Sensors	3	0	0	3
PAE16453	Digital Signal Processing Integrated Circuits	3	0	0	3
PAE16454	RF System Design	3	0	0	3
PAE16455	Solid State Device Modeling and Simulation	3	0	0	3

SEMESTER I

PMA16103 APPLIED MATHEMATICS FOR ELECTRONICS ENGINEERS 3 2 0 4

COURSE OBJECTIVES

- To gain fundamental knowledge of fuzzy sets, fuzzy logic, fuzzy decision making and fuzzy control systems.
- To focus on the concept of ordinary differential equations.
- To understand the concepts of matrix theory
- To know about dynamic programming and its applications.
- To understand and compute quantitative metrics of performance for queuing systems

UNIT I FUZZY LOGIC 15

Classical logic – Multivalued logics – Fuzzy propositions – Fuzzy quantifiers

UNIT II MATRIX THEORY 15

Generalized Eigen values and Eigen vectors - Some important matrix factorizations – The Cholesky decomposition – QR factorization – Least squares method – Singular value decomposition - Toeplitz matrices and some applications

UNIT III ORDINARY DIFFERENTIAL EQUATIONS 15

Runge - Kutta Methods for system of IVPs – Numerical stability – Adams-Bashforth multistep method – Solution of stiff ODEs – shooting method – BVP: Finite difference method, orthogonal collocation method, orthogonal collocation with finite element method, Galerkin finite element method.

UNIT IV DYNAMIC PROGRAMMING 15

Dynamic programming – Principle of optimality – Forward and backward recursion –Applications of dynamic programming – Problem of dimensionality

UNIT V QUEUING MODELS 15

Markovian queues – Single and Multi-server Models – Little's formula -Machine Interference Model – Steady State analysis – Self Service queue.

TOTAL: 75 PERIODS

COURSE OUTCOMES

At the end of this course, the students will be able to

- understand the basic principles of fuzzy logic.
- know the basics and gained the skill for specialized studies and research.
- develop efficient algorithms for solving dynamic programming problems, to acquire skills in handling situation involving random variable.
- gain knowledge in the basic characteristic features of a queuing system and acquire skills in analyzing queuing models.

REFERENCES

1. George J. Klir and Yuan, B., "Fuzzy sets and fuzzy logic, Theory and applications," Prentice Hall of India Pvt. Ltd., 1997.
2. Moon, T.K., Sterling, W.C., "Mathematical methods and algorithms for signal processing", Pearson Education, 2000.
3. Saumyen Guha and Rajesh Srivastava, "Numerical methods for Engineering and Science", Oxford Higher Education, New Delhi, 2010.
4. Taha, H.A., "Operations Research, An introduction", 7th edition, Pearson education editions, Asia, New Delhi, 2002.
5. Donald Gross and Carl M. Harris, "Fundamentals of Queuing theory", 2nd edition, John Wiley and Sons, New York (1985).

WEB LINKS

- https://www.youtube.com/watch?v=P8wY6mi1vV8
- https://www.youtube.com/watch?v=35UmpC6nrg8
- https://www.youtube.com/watch?v=RI1Ey1LkpxQ
- https://www.youtube.com/watch?v=c2DymN34w04

PAE16101 ADVANCED DIGITAL SIGNAL PROCESSING 3 2 0 4

COURSE OBJECTIVES

- To impart knowledge on multirate signal processing and FIR filter design
- To develop fundamental understanding on power spectrum estimation
- To study about linear estimation and prediction
- To impart knowledge about adaptive filters and wavelet transform

UNIT I MULTIRATE SIGNAL PROCESSING AND MULTIRATE FIR FILTER DESIGN 15

Introduction to Decimation and Interpolation -Design of FIR filters for sampling rate conversion – Applications of Interpolation and decimation in signal processing –Filter bank implementation –Two channel filter banks-QMF filter banks –Perfect Reconstruction Filter banks – tree structured filter banks

UNIT II POWER SPECTRAL ESTIMATION 15

Estimation of spectra from finite duration observations of a signal – The Periodogram - Use of DFT in Power spectral Estimation –Non-Parametric methods for Power spectrum Estimation – Bartlett Welch and Blackman–Turkey methods –Comparison of performance of Non – Parametric power spectrum Estimation methods –Parametric Methods - Yule-Walker equations, solutions using Durbin's algorithm, AR, MA, ARMA model based spectral estimation. Application: speech enhancement using power spectrum estimation

UNIT III LINEAR ESTIMATION AND PREDICTION 15

Forward and Backward linear prediction, Filtering - FIR Wiener filter- Filtering and linear prediction, non-causal and causal IIR Wiener filters, Discrete Kalman filter

UNIT IV ADAPTIVE FILTERS 15

Principles of adaptive filter – FIR adaptive filter – Newton's steepest descent algorithm – Derivation of first order adaptive filter – LMS adaptation algorithms – Adaptive noise cancellation, Adaptive equalizer, Adaptive echo cancellers

UNIT V WAVELET TRANSFORM 15

Short Time Fourier Transform, Continuous and discrete wavelet transform, Multi resolution analysis, Application of wavelet transform, Cepstrum and Homomorphic filtering

TOTAL: 75 PERIODS

COURSE OUTCOMES

At the end of this course, the students will be able to

- understand multirate signal processing
- gain knowledge about power spectrum estimation
- explain the linear estimation and prediction
- learn about adaptive filters
- analyze the wavelet transforms.

REFERENCES

1. Monson H, Hayes, “Statistical Digital Signal Processing and Modeling”, John Wiley and Sons Inc., New York, Indian Reprint, 2007.
2. Rafael C. Gonzalez, Richard E. Woods, “Digital Image Processing”, Pearson, Second Edition, 2004.
3. John G.Proakis, Dimitris G. Manolakis, “Digital Signal Processing”, Pearson, Fourth 2007.
4. Sophocles J. Orfanidis, “Optimum Signal Processing - An Introduction”, McGraw Hill, 1990.

WEB LINKS

1. www.gwyddion.net/documentation/user-guide-en/wavelet-transform.html
2. www.nptel.ac.in/courses/108105059/12
3. www.nptel.ac.in/courses/117101001

PAE16102 ADVANCED DIGITAL LOGIC SYSTEM DESIGN 3 2 0 4

COURSE OBJECTIVES

- To familiarize the practical issues of sequential circuit design
- To understand the concepts of Asynchronous Sequential Circuit Design.
- To study the concepts & gain knowledge about different fault diagnosis and testing methods.
- To design & timing Analysis of PLD's and FPGA
- To study the performance estimation of digital systems.

UNIT I SEQUENTIAL CIRCUIT DESIGN 15

Analysis of Clocked Synchronous Sequential Networks (CSSN) - Modeling of CSSN – State Assignment and Reduction – Design of CSSN – Design of Iterative Circuits– ASM Chart – ASM Realization, Design of Arithmetic circuits for Fast adder- Array Multiplier

UNIT II ASYNCHRONOUS SEQUENTIAL CIRCUIT DESIGN 15

Analysis of Asynchronous Sequential Circuit (ASC) – Flow Table Reduction – Races in ASC – State Assignment Problem and the Transition Table – Design of ASC – Static and Dynamic Hazards – Essential Hazards – Design of Hazard free circuits - Data Synchronizers –Designing Vending Machine Controller – Mixed Operating Mode Asynchronous Circuits. Practical issues such as clock skew, synchronous and asynchronous inputs and switch bouncing

UNIT III FAULT DIAGNOSIS AND TESTING 15

Fault diagnosis: Fault Table Method – Path Sensitization Method – Boolean Difference Method –Kohavi Algorithm – Tolerance Techniques – The Compact Algorithm. Design for testability: Test Generation – Masking Cycle – DFT Schemes. Circuit testing fault model, specific and random faults, testing of sequential circuits, Built-in Self-Test, Built in Logic Block observer (BILBO), signature analysis.

UNIT IV SYNCHRONOUS DESIGN USING PROGRAMMABLE DEVICES 15

EPROM to Realize a Sequential Circuit – Programmable Logic Devices – Designing a Synchronous Sequential Circuit using a GAL – EPROM – Realization State machine using PLD – FPGA – Xilinx FPGA– Xilinx 2000 -Xilinx 3000

UNIT V SYSTEM DESIGN USING VHDL 15

VHDL Description of Combinational Circuits – Arrays – VHDL Operators – Compilation and Simulation of VHDL Code – Modeling using VHDL – Flip Flops – Registers – Counters – Sequential Machine –Combinational Logic Circuits - VHDL Code for – Serial Adder, Binary Multiplier – Binary Divider –complete Sequential Systems – Design of a Simple Microprocessor

TOTAL: 75 PERIODS

COURSE OUTCOMES

At the end of this course, the students will be able to

- understand the synchronous sequential circuit design

- design asynchronous sequential circuit design
- know about the fault diagnosis& testing methods
- design and timing analysis of PLD's and FPGA
- study the performance and estimation of digital systems.

REFERENCES

1. Charles H.Roth, "Fundamentals of Logic Design", Thomson Learning 2004.
2. ParagK.Lala "An introduction to Logic Circuit Testing", Morgan and claypool publishers, 2009.
3. J.F.Wakerly, "Digital Design principles and practices", PHI publications, 2005.
4. G.DonaldGivone, "Digital principles and Design", Tata McGraw Hill 2002.
5. H.Charles Roth, "Digital System Design using VHDL", Thomson Learning, 2007.

WEB LINKS

1. www.nptel.ac.in/video.php?subjectId=117106086
2. www.wiley.com
3. www.nptel.ac.in/courses/117105080/21

PAE16103 ADVANCED MICROPROCESSOR AND MICROCONTROLLER 3 2 0 4

COURSE OBJECTIVES

- To expose the students to the fundamentals of microprocessor architecture.
- To introduce the advanced features in microprocessors and microcontrollers.
- To enable the students to understand various microcontroller architectures
- To understand in built function of PIC controller.
- To understand about special purpose processors.

UNIT I MICROPROCESSOR ARCHITECTURE 15

Instruction set – Data formats – Instruction formats – Addressing modes – Memory hierarchy – register file Cache – Virtual memory and paging – Segmentation – Pipelining – The instruction pipeline – pipeline Hazards- The software model – functional description – CPU pin descriptions – RISC concepts – RISC Properties – RISC Evaluation- RISC Versus CISC- Virtual 8086 model – Interrupt processing - Instruction types – Addressing modes – Processor flags – Instruction set

UNIT II HIGH PERFORMANCE CISC ARCHITECTURE-PENTIUM 15

CPU Architecture- Bus Operations – Pipelining – Brach predication – floating point unit-Operating Modes –Paging – Multitasking – Exception and Interrupts – Instruction set –addressing modes – Programming the Pentium processor.

UNIT III HIGH PERFORMANCE RISC ARCHITECTURE-ARM 15

Organization of CPU – Bus architecture –Memory management unit - ARM instruction set- Thumb Instruction set- addressing modes – Programming the ARM processor.6

UNIT IV PIC MICRO-CONTROLLER 15

CPU Architecture – Instruction set – interrupts- Timers- I2C Interfacing – UART- A/D Converter – PWM and introduction to C-Compilers

UNIT V SPECIAL PURPOSE PROCESSORS 15

Altera Cyclone Processor – Audio codec – Video codec design- Platforms-General Purpose processor- Digital Signal Processor – Embedded Processor- Media Processor – Video Signal Processor- Custom Hardware-CO-Processor

TOTAL: 75 PERIODS

COURSE OUTCOMES

At the end of this course, the students will be able to

- design and implement of advanced microprocessors
- know about the high performance RISC and CISC architecture
- perform PIC microcontroller programming
- know about the various special purpose processors.

REFERENCES

1. Gene .H.Miller, “Micro Computer Engineering”, Pearson Education, 2003.
2. Steve Furber, “ARM System –On –Chip architecture”, Addision Wesley, 2000.
3. John .B.Peatman, “Design with PIC Microcontroller”, Prentice hall, 1997.
4. James L.Antonakos, “An Introduction to the Intel family of Microprocessors”, Pearson Education 1999.
5. Iain E.G.Richardson, “Video Codec Design”, John Wiley & Sons ltd, U.K, 2002.

WEB LINKS

1. www.advancedmsinc.com
2. www.sciencedirect.com/science/book/9780124518308
3. www.arm.com

PAE16104 MULTICORE ARCHITECTURE AND PROGRAMMING 3 2 0 4

COURSE OBJECTIVES

- To introduce the recent trends in the field of multicore processor.
- To understand the challenges in parallel and multi-threaded programming.
- To learn about the various parallel programming paradigms, and solutions.

UNIT I MULTI-CORE PROCESS 15

Single core to Multi-core architectures – SIMD and MIMD systems – Interconnection networks - Symmetric and Distributed Shared Memory Architectures – Cache coherence- Performance Issues – Parallel program design.

UNIT II PARALLEL PROGRAM CHALLENGES 15

Performance – Scalability – Synchronization and data sharing – Data races – Synchronization primitives (mutexes, locks, semaphores, barriers) – deadlocks and live locks – communication between threads (condition variables, signals, message queues and pipes)

UNIT III SHARED MEMORY PROGRAMMING WITH OPEN MP 15

Open MP Execution Model – Memory Model – Open MP Directives – Work-sharing Constructs – Library functions – Handling Data and Functional Parallelism – Handling Loops – Performance Considerations.

UNIT IV DISTRIBUTED MEMORY PROGRAMMING WITH MPI 15

MPI program execution – MPI constructs – libraries – MPI send and receive – Point-to-point and Collective communication – MPI derived data types – Performance evaluation

UNIT V PARALLEL PROGRAM DEVELOPMENT 15

Case studies - n-Body solvers – Tree Search – Open MP and MPI implementations and comparison.

TOTAL: 75 PERIODS

COURSE OUTCOMES

At the end of this course, the students will be able to

- program parallel processors.
- develop programs using open mp and MPI.
- compare and contrast programming for serial processors and programming for parallel processors.

REFERENCES

1. Michael J Quinn, “Parallel programming in C with MPI and Open MP”, Tata McGraw Hill, 2003.
2. Peter S. Pacheco, “An Introduction to Parallel Programming”, Morgan Kauffman/Elsevier, 2011.

3. Darryl Gove, “Multicore Application Programming for Windows, Linux, and Oracle Solaris”, Pearson, 2011
4. John L. Hennessey and David A. Patterson, “Computer Architecture – A Quantitative Approach”, Morgan Kaufmann / Elsevier, 5th edition, 2012.
5. Kai Hwang, “Advanced Computer Architecture”, Tata McGraw-Hill Education, 2003.

WEB LINKS

1. www.nptel.ac.in/courses/106104025
2. https://software.intel.com
3. www.springer.com/us/book/9783540245605

PAE16105 ELECTRONICS SYSTEM DESIGN LABORATORY I 0 0 4 2

COURSE OBJECTIVES

- To know and understand microcontroller and design circuits using it.
- To write programs in VHDL and Verilog for modeling digital circuits
- To study and verify the combinational and sequential logic circuits with various levels of modeling and EDA Tools.

LIST OF EXPERIMENTS

1. To write programs in VHDL and Verilog for modeling digital circuits
2. System design using PIC, MSP430, ‘51 Microcontroller and 16- bit Microprocessor - 8086.
3. Implementation of Adaptive Filters in DSP Processor
4. Implementation of multistage multirate system in DSP Processor
5. Simulation of QMF using Simulation Packages
6. Analysis of Asynchronous clocked sequential circuits
7. Analysis of synchronous clocked sequential circuits
8. Sensor design using simulation tools
9. Design and analysis of real time signal processing system – Data acquisition and signal processing.
10. Timer Operation – Real Time Clock using ARM processor

TOTAL: 60 PERIODS

COURSE OUTCOMES

At the end of this course, the students will be able to

- make models of transistor circuits and simulate them for various operational requirements.
- design different types of multiplier using EDA tool.
- design FIR filter using EDA tool.
- analyze and design of VLSI circuits.

SEMESTER II

PAE16201 ANALYSIS AND DESIGN OF ANALOG INTEGRATED CIRCUITS 3 2 0 4

COURSE OBJECTIVES

- To impart knowledge in the CMOS Technology and modeling of devices
- To understand the basic concepts of CMOS operational amplifiers
- To find the optimum solution for the complex problem in multistage amplifier.
- To study the stability and frequency compensation techniques.
- To acquire the knowledge about biasing circuit.

UNIT I CMOS TECHNOLOGY AND DEVICE MODELING 15

Basic MOS semiconductor fabrication processes-other considerations of CMOS technology-MOS large signal model and parameters-Small signal model for the MOS transistor-Computer simulation models-Sub threshold MOS model.

UNIT II FREQUENCY RESPONSE AND NOISE ANALYSIS 15

Miller effect, Association of poles with nodes, frequency response of common source stage, Source followers, Common gate stage, Cascode stage, Differential pair, Statistical characteristics of noise -noise in single stage amplifiers, noise in differential amplifiers.

UNIT III CMOS OPERATIONAL AMPLIFIERS 15

Buffered operational amplifiers-High speed and frequency operational amplifiers-Differential output operational amplifiers-Microwave operational amplifiers - Low noise operational amplifiers - Low voltage operational amplifiers.

UNIT IV STABILITY AND FREQUENCY COMPENSATION 15

General considerations, Multipole systems, Phase Margin, Frequency Compensation, and Compensation of two stage Op Amps, Slewing in two stage Op Amps, and Other compensation techniques.

UNIT V BIASING CIRCUITS 15

Basic current mirrors, cascode current mirrors, active current mirrors, voltage references, supply independent biasing, temperature independent references, PTAT current generation, Constant-Gm biasing.

TOTAL: 75 PERIODS

COURSE OUTCOMES

At the end of this course, the students will be able to

- gain knowledge in CMOS technology and device modeling
- perform analysis on frequency response and noise
- understand CMOS operational amplifiers.
- understand the stability and frequency compensation techniques.
- know about biasing circuits.

REFERENCES

1. Paul R. Gray, Paul J. Hurst, Stephen H. Lewis, Robert G. Meyer, "Analysis and Design of Analog Integrated Circuits", 5th Edition, Wiley, 2009.
2. Behzad Razavi, "Design of Analog CMOS Integrated Circuits", Tata McGraw Hill, 2001.
3. Willey M.C. Sansen, "Analog design essentials", Springer, 2006.
4. Grebene, "Bipolar and MOS Analog Integrated circuit design", John Wiley & sons, Inc., 2003.
5. Phillip E.Allen, Douglas R.Holberg, "CMOS Analog Circuit Design", Second edition, Oxford University Press, 2002 .

WEB LINKS

1. www.wiley.com
2. www.nptelvideos.in/2012/12/electronics.html
3. www.nptel.ac.in/syllabus/117105027

PAE16202 ASIC AND FPGA DESIGN 3 2 0 4

COURSE OBJECTIVES

- To learn the fundamentals of ASIC and its design methods and the physical design of ASIC.
- To learn logic synthesis and testing.
- To gain knowledge in programmable architectures for ASICs.
- To learn the concepts of system on chip design.

UNIT I OVERVIEW OF ASIC AND PLA 15

Types of ASICs - Design flow – CAD tools used in ASIC Design – Programming Technologies: Anti fuse – static RAM – EPROM and EEPROM technology, Programmable Logic Devices: ROMs and EPROMs – PLA –PAL. Gate Arrays – CPLDs and FPGAs

UNIT II ASIC PHYSICAL DESIGN PROGRAMMABLE ASIC 15

System partition -partitioning - partitioning methods – interconnect delay models and measurement of delay - floor planning - placement – Routing: global routing - detailed routing - special routing – circuit extraction – DRC. Anti fuse -Static RAM - EPROM and EEPROM technology – Practical issues - PREP benchmarks - Actel ACT - Xilinx LCA –Altera FLEX - Altera MAX – Xilinx Spartan – Virtex FPGAs – Altera Cyclone FPGAs

UNIT III LOGIC SYNTHESIS AND SIMULATION TESTING 15

Design systems - Logic Synthesis - Half gate ASIC -Schematic entry - Low level design language -PLA tools -EDIF- CFI design representation. Verilog and logic synthesis -VHDL and logic synthesis -types of simulation -boundary scan test - fault simulation - automatic test pattern generation

UNIT IV FPGA ARCHITECTURE 15

Field Programmable gate arrays- Logic blocks, routing architecture, Design flow technology – mapping for FPGAs, Xilinx XC4000 - ALTERA's FLEX 8000/10000, ACTEL's ACT-1,2,3 and their speed performance Case studies: Altera MAX 5000 and 7000 - Altera MAX 9000 – Spartan II and Virtex II FPGAs – Apex and Cyclone FPGAs

UNIT V SOC DESIGN 15

Design Methodologies – Processes and Flows - Embedded software development for SOC –Techniques for SOC Testing – Configurable SOC – Hardware / Software co-design Case studies: Digital camera, Bluetooth radio / modem, SDRAM and USB.

TOTAL: 75 PERIODS

COURSE OUTCOMES

At the end of this course, the students will be able to

- understand different types of ASIC's and physical design of ASIC.
- understand logic synthesis and testing methods and different FPGA architectures.
- design real time applications on SOC.

REFERENCES

1. M.J.S .Smith, "Application Specific Integrated Circuits", Addison -Wesley Longman Inc., 1997
2. R. Rajsuman, "System-on-a-Chip Design and Test", Santa Clara, CA: Artech House Publishers, 2000.
3. S.Trimberger, "Field Programmable Gate Array Technology", Edr, Kluwer Academic Publications, 1994.
4. John V.Oldfield, Richard C Dore, "Field Programmable Gate Arrays", Wiley Publications1995.
5. P.K.Chan & S. Mourad, "Digital Design Using Field Programmable Gate Array", Prentice Hall, 1994.

WEB LINKS

1. www.eetimes.com/author.asp?section_id=36&doc_id=1322856
2. www.eeherald.com/section/design-guide/dg100009.html
3. www.differencebetween.net

PAE16203 LOW POWER VLSI DESIGN 3 2 0 4

COURSE OBJECTIVES

- To know the sources of power consumption in CMOS circuits
- To understand the various power reduction techniques and the power estimation methods.
- To study the design concepts of low power circuits.

UNIT I POWER DISSIPATION IN CMOS 15

Hierarchy of limits of power – Sources of power consumption – Physics of power dissipation in CMOS FET devices- Basic principle of low power design.

UNIT II POWER OPTIMIZATION 15

Logical level power optimization – Circuit level low power design – Circuit techniques for reducing power consumption in adders and multipliers - CMOS Circuits design styles, Adders, Multipliers

UNIT III DESIGN OF LOW POWER CMOS CIRCUITS 15

Computer Arithmetic techniques for low power systems – Reducing power consumption in memories – Low power clock, Interconnect and layout design – Advanced techniques – Special techniques

UNIT IV POWER ESTIMATION 15

Power estimation techniques – Logic level power estimation – Simulation power analysis – Probabilistic power analysis- Random Logic signals – Probabilistic power analysis techniques

UNIT V SYNTHESIS AND SOFTWARE DESIGN FOR LOW POWER 15

Synthesis for low power –Behavioral level transforms- Software design for low power – Sources of software power Dissipation – Software Power Estimation –Software Power optimization

TOTAL: 75 PERIODS

COURSE OUTCOMES

At the end of this course, the students will be able to

- know the basic concepts and principles of CMOS
- understand the techniques of reducing power consumption
- know about advanced and special techniques for low power systems
- gain knowledge in the techniques involved in power estimation
- design software for low power

REFERENCES

1. K.Roy and S.C. Prasad, “Low Power CMOS VLSI circuit design”, Wiley, 2000
2. Dimitrios Soudris, Chirstian Pignet, Costas Goutis, “Designing CMOS Circuits For Low Power”, Kluwer, 2002
3. J.B. Kuo and J.H Lou, “Low voltage CMOS VLSI Circuits”, Wiley 1999.
4. Gary Yeap, “Practical low power digital VLSI design”, Kluwer, 1998.

5. James B. Kuo, Shin – chia Lin, “Low voltage SOI CMOS VLSI Devices and Circuits”, John Wiley and sons, Inc 2001.

WEB LINKS

1. www.nptel.ac.in/courses/106105034
2. www.worldscientific.com
3. www.powershow.com/.

PAE16207 ELECTRONICS SYSTEM DESIGN LABORATORY II 0 0 4 2

COURSE OBJECTIVES

- To learn the fundamentals of real time operating systems.
- To gain knowledge on VHDL and Verilog HDL.
- To learn flash controller programming.
- To design implementation of digital logic using FPGA.

LIST OF EXPERIMENTS

1. Design and Simulation of CMOS Memory Cell using SPICE. Testing RTOS environment and system programming
2. Design and Simulation of NMOS and CMOS Logic Gates using SPICE
3. Designing of wireless network using embedded systems
4. Implementation of ARM with FPGA
5. Design and Implementation of ALU in FPGA using VHDL and Verilog
6. Modeling of Sequential Digital system using Verilog and VHDL
7. Flash controller programming - data flash with erase, verify and fusing
8. System design using ASIC
9. Design, simulation and analysis of signal integrity.
10. Mini Project

TOTAL: 60 PERIODS

COURSE OUTCOMES

At the end of this course, the students will be able to

- understand RTOS and microcontroller.
- design and check flash controller program.
- understand wireless data transmission
- design a system using ASIC
- design and implementation of digital circuits using FPGA.

ELECTIVE I

PAE16151 ADVANCED DIGITAL IMAGE PROCESSING 3 0 0 3

COURSE OBJECTIVES

- To introduce the basics of digital image processing.
- To learn applications of segmentation with texture analysis
- To introduce theory of feature extraction
- To acquire the concept of image fusion
- To study the applications of image processing

UNIT I FUNDAMENTALS OF DIGITAL IMAGE PROCESSING 9

Elements of visual perception, brightness, contrast, hue, saturation, mach band effect, 2D image transforms-DFT, DCT, KLT, and SVD. Image enhancement in spatial and frequency domain, Review of morphological image processing

UNIT II SEGMENTATION AND TEXTURE ANALYSIS 9

Edge Linking and Boundary Detection - Local Processing-Global Processing –Thresholding-Segmentation by Morphological Watershed Segmentation Algorithm - Use of Markers- Use of Motion in Segmentation-Spatial Techniques-Frequency Domain Techniques-Texture- Statistical, Syntactic and Hybrid texture description - texture recognition and applications

UNIT III FEATURE EXTRACTION 9

First and second order edge detection operators, Phase congruency, Localized feature extraction detecting image curvature, shape features Hough transform, shape skeletonization, Boundary descriptors, Moments, Texture descriptors- Autocorrelation, Co-occurrence features, Run length features, Fractal model based features, Gabor filter, wavelet features

UNIT IV REGISTRATION AND IMAGE FUSION 9

Registration- Preprocessing, Feature selection-points, lines, regions and templates Feature correspondence-Point pattern matching, Line matching, and region matching Template matching. Transformation functions-Similarity transformation and Affine Transformation - Resampling- Nearest Neighbor and Cubic Splines Image Fusion-Overview of image fusion, pixel fusion, Multiresolution based fusion discrete wavelet transform, Curvelet transform - Region based fusion.

UNIT V IMAGE PROCESSING APPLICATIONS 9

Image compression- JPEG, JPEG2000 and MPEG standards- Watermarking-Steganography-3D vision tasks- Marr’s theory, active and purposive vision- Geometry for 3D vision-Use of 3D vision-Shape from X-shape - motion, texture- Full 3D objects.

TOTAL: 45 PERIODS

COURSE OUTCOMES

At the end of this course, the students will be able to

- know the basic concepts of image processing

- understand the working and applications of segmentation.
- apply 3D image visualization and image processing applications
- gain knowledge about working of image fusion

REFERNCES

1. John C.Russ, “The Image Processing Handbook”, CRC Press, 2007.
2. Mark Nixon, Alberto Aguado, “Feature Extraction and Image Processing”, Academic Press, 2008.
3. Ardeshir Goshtasby, “2D and 3D Image registration for Medical, Remote Sensing and Industrial Applications”, John Wiley and Sons, 2005.
4. H.B.Mitchell, “Image Fusion Theories, Techniques and Applications”, Springer, 2010.
5. Rafael C. Gonzalez, Richard E. Woods, “Digital Image Processing”, Pearson, Education, Inc., Second Edition, 2004.

WEB LINKS

1. www.springer.com/us/book/9781848829183
2. http://www.eng.tau.ac.il/~yaro/lectnotes
3. www.nptel.ac.in/courses/117105079

PAE16152 WAVELET TRANSFORMS AND APPLICATIONS 3 0 0 3

COURSE OBJECTIVES

- To understand the fundamentals of vector analysis.
- To learn the concepts of multi resolution analysis.
- To study the properties of continuous wavelet transforms.
- To characterize filter bank and sub band coding principles.
- To study the various image compression techniques.

UNIT I MATHEMATICAL FUNDAMENTALS 9

Linear spaces – Vectors and vector spaces – Basis functions – Dimensions –Orthogonality and bio-rthogonalilty– Local basis and Riesz basis – Discrete linear normed space – Approximation by orthogonal projection –Matrix algebra and linear transformation..

UNIT II MULTI RESOLUTION ANALYSIS 9

Definition of Multi Resolution Analysis (MRA) – Haar Basis – Construction of General Orthonormal MRA – Wavelet Basis for MRA – Continuous Time MRA Interpretation for the DTWT – Discrete Time MRA – Basis Functions for the DTWT – PRQMF Filter Banks.

UNIT III CONTINUOUS WAVELET TRANSFORMS 9

Wavelet Transform – Definition and Properties – Concept of Scale and its Relation with Frequency – Continuous Wavelet Transform (CWT) – Scaling Function and Wavelet Functions (Daubechies Coiflet, Mexican Hat, Sinc, Gaussian, Bi Orthogonal) – Tiling of Time – Scale Plane for CWT.

UNIT IV DISCRETE WAVELET TRANSFORMS 9

Filter Bank and Sub Band Coding Principles – Wavelet Filters – Inverse DWT Computation by Filter Banks – Basic Properties of Filter Coefficients – Choice of Wavelet Function Coefficients – Derivations of Daubechies Wavelets – Mallat's Algorithm for DWT – Multi Band Wavelet Transforms Lifting Scheme- Wavelet Transform Using Poly phase Matrix Factorization.

UNIT V TRANSFORMS AND ITS APPLICATIONS 9

Wavelet methods for signal processing- Image Compression Techniques: EZW–SPHIT Coding –Image Denoising Techniques: Noise Estimation – Shrinkage Rules – Shrinkage Functions – Edge Detection and Object Isolation, Image Fusion, and Object Detection.

TOTAL: 45 PERIODS

COURSE OUTCOMES

At the end of this course, the students will be able to

- apply the fundamentals of vector analysis.
- know the concepts of multi resolution analysis.
- understand the properties of continuous wavelet transforms.
- apply the knowledge of filter bank and sub band coding principles.
- understand the various image compression techniques.

REFERENCES

1. Rao R.M and A.S.Bopardikar, “Wavelet Transforms Introduction to theory and Applications”, Pearson Education, Asia, 2000.
2. J.C.Goswami and A. K. Chan, “Fundamentals of wavelets: Theory, Algorithms and Applications", Wiley Inter science Publication, John Wiley & Sons Inc., 1999.
3. M. Vetterli, J.Kovacevic, “Wavelets and subband coding", Prentice Hall Inc, 1995.
4. Stephen G. Mallat, “A wavelet tour of signal processing", 2nd Edition Academic Press, 2000.
5. Soman K.P and Ramachandran K.I, “Insight into Wavelets from Theory to practice”, Prentice Hall, 2004.

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PAE16153 PHYSICAL DESIGN OF VLSI CIRCUITS 3 0 0 3

COURSE OBJECTIVES

- To gain knowledge in the basic rules of layout and cell generations.
- To study about the placement and floor sizing.
- To learn about the multiple partition, routing and how to increases the layout performance.
- To improve the performance in the layout design.
- To acquire knowledge about cell partition and generation.

UNIT I REVIEW OF VLSI TECHNOLOGY 9

Layout Rules-Circuit abstraction Cell generation using programmable logic array transistor chaining, Wein Berger arrays and gate matrices-layout of standard cells gate arrays and sea of gates, field programmable gate array(FPGA)-layout methodologies Packaging-Computational Complexity-Algorithmic Paradigms

UNIT II PLACEMENT USING TOP-DOWN APPROACH 9

Partitioning: Approximation of Hyper Graphs with Graphs, Kernighan-Lin Heuristic Ratio cut- partition with capacity and i/o constraints. Floor planning: Rectangular dual floor planning- hierarchical approach simulated annealing- Floor plan sizing Placement: Cost function- force directed method- placement by simulated annealing partitioning placement- module placement on a resistive network – regular placement linear placement.

UNIT III ROUTING USING TOP DOWN APPROACH 9

Fundamentals: Maze Running- line searching- Steiner trees Global Routing: Sequential Approaches hierarchical approaches- multi commodity flow based techniques- Randomized Routing- One Step approach- Integer Linear Programming Detailed Routing: Channel Routing- Switch box routing. Routing in FPGA: Array based FPGA- Row based FPGAs

UNIT IV PERFORMANCE ISSUES IN CIRCUIT LAYOUT 9

Delay Models: Gate Delay Models- Models for interconnected Delay- Delay in RC trees. Timing – Driven Placement: Zero Stack Algorithm- Weight based placement- Linear Programming Approach Timing riving Routing: Delay Minimization- Click Skew Problem- Buffered Clock Trees. Minimization: constrained via Minimization unconstrained via Minimization- Other issues in minimization

UNIT V LAYOUT DESIGN AND TOOLS 9

Transistor structures, Wires and Vias, Scalable Design rules, Layout Design tools. Logic Gates & Layouts: Static Complementary Gates, Switch Logic, Alternative Gate circuits, Low power gates, Resistive and Inductive interconnect delays.

TOTAL: 45 PERIODS

COURSE OUTCOMES

At the end of this course, the students will be able to

- design, simulate, built an abstract functional specification.
- do partition in the layout easily for the design of PCB boards in accurate manner using many approaches.
- discover the debug complex combinational and sequential circuits based on an abstract functional specification.
- perform the cell partition and generation.
- formulate the routing of the cell.

REFERENCES

1. Sarafzadeh, C.K. Wong, "An Introduction to VLSI Physical Design", McGraw Hill International Edition 1995
2. Preas M. Lorenzatti, "Physical Design and Automation of VLSI systems", The Benjamin Cummins Publishers, 1998.
3. Jose E. France and Yannis T sividis, "Design of Analog - Digital VLSI Circuits for Telecommunication and Signal Processing", Prentice Hall, 1994.
4. Thomas H.Lee, "The Design of CMOS Radio –Frequency Integrated Circuits", Cambridge University Press , 2003

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PAE16154 COMPUTER ARCHITECTURE AND PARALLEL PROCESSING 3 0 0 3

COURSE OBJECTIVES

- To know the basics of computer design and performance measures
- To introduce the concepts of parallel processing and pipelining
- To educate about hardware technologies
- To gain knowledge about multiprocessors
- To introduce Multicore architectures

UNIT I THEORY OF PARALLELISM 9

Fundamentals of Computer Design – Parallel and Scalable Architectures – Multiprocessors – Multi vector and SIMD architectures – Multithreaded architectures – Data-flow architectures - Performance Measures

UNIT II PARALLEL PROCESSING, PIPELINING AND ILP 9

Instruction Level Parallelism and Its Exploitation - Concepts and Challenges - Overcoming Data Hazards with Dynamic Scheduling – Dynamic Branch Prediction - Speculation - Multiple Issue Processors - Performance and Efficiency in Advanced Multiple Issue Processors

UNIT III HARDWARE TECHNOLOGIES 9

Processor and memory hierarchy advanced processor technology, superscalar and vector processors, memory hierarchy technology, virtual memory technology- Bus cache and Shared Memory - backplane bus systems, cache memory organizations, shared memory organizations, sequential and weak consistency models, Pipelining and superscalar Techniques.

UNIT IV MULTIPROCESSORS 9

Symmetric and distributed shared memory architectures – Cache coherence issues – Performance Issues – Synchronization issues – Models of Memory Consistency - Interconnection networks – Buses, crossbar and multi-stage switches.

UNIT V MULTI-CORE ARCHITECTURES 9

Software and hardware multithreading – SMT and CMP architectures – Design issues – Case studies – Intel Multi-core architecture – SUN CMP architecture – IBM cell architecture - hp architecture.

TOTAL: 45 PERIODS

COURSE OUTCOMES

At the end of this course, the students will be able to

- understand the computer design concepts
- understand the parallel processing and pipelining
- gain knowledge in memory hierarchy design
- know about multiprocessors and the multi-core architecture

REFERENCES

1. Kai Hwang, "Advanced Computer Architecture", McGraw Hill International, 2001.
2. John L. Hennessey and David A. Patterson, “Computer Architecture – A quantitative approach”, Morgan Kaufmann / Elsevier, 4th. Edition, 2007.
3. William Stallings, “Computer Organization and Architecture – Designing for Performance”, Pearson Education, Seventh Edition, 2006.
4. John P. Hayes, “Computer Architecture and Organization”, McGraw Hill
5. David E. Culler, Jaswinder Pal Singh, “Parallel Computing Architecture: A hardware/ software approach”, Morgan Kaufmann / Elsevier, 1997.

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ELECTIVE II

PAE16251 CAD FOR VLSI CIRCUITS 3 0 0 3

COURSE OBJECTIVES

- To introduce the basic CAD algorithm and partitioning
- To educate about the placement, floor planning
- To learn about global, detail routing
- To know the modeling and synthesis in CAD flow.

UNIT I LOGIC SYNTHESIS & BASIC CAD ALGORITHMS 9

Introduction to combinational logic synthesis - Binary Decision Diagram - Hardware models for High-level synthesis - graph algorithms - computational geometry algorithms.

UNIT II PARTITIONING 9

Classification of partitioning algorithms - Group migration algorithms - simulated annealing & evolution, other partitioning algorithms

UNIT III PLACEMENT, FLOOR PLANNING & PIN ASSIGNMENT 9

Simulation base placement algorithms, other placement algorithms - constraint based floor planning - floor planning algorithms for mixed block & cell design - General & channel pin assignment for register minimization, Global routing - Algorithms for global routing

UNIT IV ROUTING 9

Classification of global routing algorithms - Maze routing algorithm - line probe algorithm - Steiner Tree based algorithms - ILP based approaches-classification of routing algorithms - single layer routing algorithms, two layer channel routing algorithms, three layer channel routing algorithms, and switchbox routing algorithms.

UNIT V SYSTEM MODELING ALGORITHMS 9

High level Synthesis - Hardware models - Internal representation - Allocation - Assignment and scheduling - Simple scheduling algorithm - Assignment problem – High level transformations

TOTAL: 45 PERIODS

COURSE OUTCOMES

At the end of this course, the students will be able to

- explain the fundamentals of basic algorithm in cad.
- analyze the different partitioning algorithm.
- know the floor planning and placement algorithm.
- understand the different routing algorithms, modeling and synthesis techniques of CAD.

REFERENCES

1. S.H. Gerez, "Algorithms for VLSI Design Automation", JohnWiley & Sons, 2002.
2. N.A. Sherwani, "Algorithms for VLSI Physical Design Automation", Kluwer Academic Publishers, 2002.
3. Sadiq M. Sait, Habib Youssef, “VLSI Physical Design automation: Theory and Practice”, World scientific 1999.

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3. www.ece.mtu.edu/~zhuofeng/EE5780Fall2013.html

PAE16252 DIGITAL CONTROL ENGINEERING 3 0 0 3

COURSE OBJECTIVES

- To impart knowledge in continuous time systems and controllers
- To develop the fundamental understanding on signal processing in digital control
- To study the design of digital control algorithms
- To impart knowledge about state variable techniques
- To give an insight knowledge about the controllability, observability and stability

UNIT I CONTINUOUS TIME SYSTEMS 9

Review of frequency and time response analysis and specifications of control systems, need for controllers, continuous time compensations, continuous time PI, PD, PID controllers.

UNIT II SIGNAL PROCESSING IN DIGITAL CONTROL 9

Sampling, time and frequency domain descriptions, aliasing, hold operations, mathematical model of sample and hold, zero and first order hold, factors limiting the choice of sample rate, reconstruction, Difference equation description, Z-transform method of description, pulse transfer function, time and frequency response of discrete time control systems.

UNIT III DESIGN OF DIGITAL CONTROL ALGORITHMS 9

Review of principle of compensator design, Z-plane specifications, digital compensator design using frequency response plots, discrete integrator, discrete differentiator, development of digital PID controller, transfer function, design in Z plane.

UNIT IV STATE VARIABLE TECHNIQUES 9

Discrete State Variable concepts, Characteristic equation, Eigen values and Eigenvectors, Jordan canonical models, Phase Variable companion forms

UNIT V CONTROLLABILITY, OBSERVABILITY AND STABILITY 9

Definitions and Theorems of Controllability and Observability, Relationships between Controllability, Observability and Transfer Functions, Jury, Routh, Lyapunov stability analysis, Principles of state and output feedback

TOTAL: 45 PERIODS

COURSE OUTCOMES

At the end of this course, the students will be able to

- understand continuous time system controllers
- gain knowledge about signal processing in digital control
- design digital control algorithms
- apply the state variable techniques
- know about controllability, observability and stability

REFERENCES

1. Benjamin C.Kuo, “Digital Control Systems”, OXFORD University Press, II Edition, 2007
2. M.Gopal, “Digital Control and State Variable Methods”, Tata McGraw Hill, II Edition, 2007.
3. K.Ogata, “Discrete-Time Control Systems”, PHI, II Edition, 2007.
4. Gene. F.Franklin, J.D.Powell, M.Workman, “Digital Control of Dynamic Systems”, Addison-Wesley, 1990.

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PAE16253 VLSI SIGNAL PROCESSING 3 0 0 3

COURSE OBJECTIVES

- To understand the basic concepts of DSP algorithms.
- To know about the folding and unfolding concepts
- To analyze the various pipelining and parallel processing techniques.
- To acquire knowledge in the retiming and unfolding algorithms for various DSP applications.
- To analyze the concept of various filters

UNIT I INTRODUCTION TO DSP SYSTEMS 9

Introduction To DSP Systems -Typical DSP algorithms; Iteration Bound – data flow graph representations, loop bound and iteration bound, Longest path Matrix algorithm; Pipelining and parallel processing – Pipelining of FIR digital filters, parallel processing, pipelining and parallel processing for low power.

UNIT II RETIMING, FOLDING AND UNFOLDING 9

Retiming - definitions and properties of Retiming techniques; Unfolding – an algorithm for Unfolding, properties of unfolding, sample period reduction and parallel processing application; Folding – Folding transformation – Register minimizing techniques – Register minimization in folded architectures.

UNIT III FAST CONVOLUTION 9

Fast convolution – Cook-Toom algorithm, modified Cook-Took algorithm –Iterated Convolution – Cyclic Convolution; Pipelined and parallel recursive and adaptive filters – inefficient/efficient single channel interleaving, Look- Ahead pipelining in first- order IIR filters, Look-Ahead pipelining with power-of-two decomposition parallel processing of IIR filters, combined pipelining and parallel processing of IIR filters, pipelined adaptive digital filters, relaxed look-ahead, pipelined LMS adaptive filter.

UNIT IV BIT–LEVEL ARCHITECTURE AND SYSTOLIC ARRAY DESIGN 9

Bit-Level Arithmetic Architectures- parallel multipliers with sign extension, parallel carry-ripple array multipliers, parallel carry-save multiplier, 4x 4 bit Baugh- Wooley carry-save multiplication tabular form and implementation, design of Lyon's bit-serial multipliers using Horner's rule, bit-serial FIR filter, CSD representation, CSD multiplication using Horner's rule for precision improvement. Systolic array design methodology – FIR systolic Arrays – selection of scheduling vector-matrix multiplication and 2D systolic array design-Systolic design for space representations containing Delays

UNIT V PROGRAMMING DIGITAL SIGNAL PROCESSORS 9

Synchronous, Wave and asynchronous pipelining- synchronous pipelining and clocking styles, clock skew in edge-triggered single-phase clocking, two-phase clocking, wave pipelining, asynchronous pipelining bundled data versus dual rail protocol; Programming Digital Signal Processors – general architecture with important features; Low power Design – needs for low power VLSI chips, charging

and discharging capacitance, short-circuit current of an inverter, CMOS leakage current, basic principles of low power design.

TOTAL: 45 PERIODS

COURSE OUTCOMES

At the end of this course, the students will be able to

- understand the basic concepts of DSP algorithms.
- analyze pipelining and other parallel processing techniques
- perform digital signal processor programming
- know process of pipelining techniques

REFERENCES

1. Keshab K.Parhi, "VLSI Digital Signal Processing systems, Design and implementation", Wiley, Inter Science, 1999.
2. Gary Yeap, "Practical Low Power Digital VLSI Design", Kluwer Academic Publishers, 1998.
3. Mohammed Isamail and Terri Fiez, "Analog VLSI Signal and Information Processing", Mc Graw-Hill, 1994.
4. Jose E. France and Yannis T sividis, "Design of Analog - Digital VLSI Circuits for Telecommunication and Signal Processing", Prentice Hall, 1994.
5. S.Y. Kung, H.J. White House, T. Kailath, "VLSI and Modern Signal Processing", Prentice Hall, 1985.

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PAE16254 SENSORS AND SIGNAL CONDITIONING 3 0 0 3

COURSE OBJECTIVES

- To introduce the basic science of measurement
- To introduce resistive sensors
- To learn the reactive sensors and self-generating sensors
- To know about measuring devices
- To study about digital sensor and semiconductor device sensors

UNIT I CHARACTERISTICS OF MEASUREMENT SYSTEMS 9

Introduction to measurement systems: general concepts and terminology, measurement systems, sensor classification, general input-output configuration, methods of correction performance characteristics: static characteristics of measurement systems, accuracy, precision, sensitivity, other characteristics: linearity, resolution, systematic errors, random errors, dynamic characteristics of measurement systems: zero-order, first-order, and second-order measurement systems and response.

UNIT II RESISTIVE SENSORS 9

Resistive sensors: potentiometers, strain gages and types, resistive temperature detectors (RTDs), thermistors, magneto resistors, light-dependent resistors (LDRs); Signal conditioning for resistive sensors: measurement of resistance, voltage, Wheatstone bridge. Balance and deflection measurements, sensor bridge calibration and compensation instrumentation amplifiers, interference types and reduction

UNIT III REACTIVE SENSORS 9

Reactance variation and electromagnetic sensors : capacitive sensors – variable & differential, inductive sensors – reluctance variation, eddy current, linear variable differential transformers (LVDTS) , variable transformers: synchros, resolvers, inductosyn , magneto elastic sensors, electromagnetic sensors – sensors based on faraday's law, hall effect sensors, Signal conditioning for reactance variation sensors : problems and alternatives, ac bridges, carrier amplifiers – application to the LVDT, variable oscillators, resolver-to-digital and digital-to-resolver converters

UNIT IV MEASURING DEVICES 9

Capacitive Impedance and Piezoelectric Hygrometers - Differential Pressure, U-tube and ultrasonic Densitometers - pH measurement: Ion Selective Type - Radiation Fundamentals-Radiation Detectors-Radiation Thermometers - Optical Pyrometers

UNIT V DIGITAL SENSORS 9

Position encoders, variable frequency sensors-quartz digital thermometer, SAW sensors, digital flow meters, sensors based on semiconductor junctions: thermometers based on semiconductor junctions, magneto diodes and magneto transistors, photodiodes and phototransistors, charge-coupled sensors.

TOTAL: 45 PERIODS

COURSE OUTCOMES

At the end of this course, the students will be able to

- gain knowledge in basic characteristics of measurement systems
- know the functionality of resistive sensors and reactive sensors
- understand the digital sensor and semiconductor device sensors

REFERENCES

1. Ramon Pallas Areny, John G. Webster, "Sensors and Signal Conditioning", 2nd edition, John Wiley and Sons, 2000.
2. D.Patranabis, "Sensors and Transducers", TMH 2003.
3. Jon Wilson, "Sensor Technology Handbook", Newnes, 2004.
4. Herman K.P. Neubrat, "Instrument Transducers – An Introduction to Their Performance and Design", Oxford University Press.
5. E.O. Doeblin, "Measurement System: Applications and Design", McGraw Hill Publications.

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3. www.freevideolectures.com

ELECTIVE III

PAE16351 MOBILE NETWORKS 3 0 0 3

COURSE OBJECTIVES

- To study the architecture and characteristics in cellular networks
- To explore enabling wireless technologies with mobile networks
- To understand Mobile IP and TCP protocols
- To explore the issues and challenges in multicast routing in ad-hoc networks

UNIT I CELLULAR CONCEPT 9

Introduction – Frequency reuse – Channel assignment strategies – Handoff strategies – Interference – Truncking – Improving coverage and capacity in cellular systems.

UNIT II WIRELESS LAN 9

Infrared vs. radio transmission- Infrastructure and Ad-hoc network – IEEE 802.11 – HIPERLAN – Bluetooth.

UNIT III MOBILE NETWORK LAYER 9

Mobile IP : Goals – Assumptions and Requirement – Entities – IP packet Delivery- Agent advertisement and Discovery – Registration – Tunneling and Encapsulation – Optimization – Reverse Tunneling – IPv6 – DHCP- Ad hoc Networks

UNIT IV MOBILE TRANSPORT LAYER 9

Traditional TCP- Indirect TCP- Snooping TCP- Mobile TCP- Fast retransmit/ Fast Recovery- Transmission/ Timeout Freezing – Selective Retransmission- Transaction Oriented TCP , TCP over 2.5/3G wireless networks.

UNIT V MULTICAST ROUTING IN AD-HOC WIRELESS NETWORKS 9

Introduction – Issues in designing a multicast routing protocol – Operations of multicast routing protocols-Tree based multicast routing protocols – Mesh based multicast routing protocol – Application Dependent multicast routing.

TOTAL: 45 PERIODS

COURSE OUTCOMES

At the end of this course, the students will be able to

- identify the various challenges and vulnerabilities in cellular networks
- understand and recognize techniques of various wireless technologies
- analyze the solutions for configuration of mobile networks
- know TCP protocols in mobile environment
- analyze the solutions for multicast routing protocols for different applications.

REFERENCES

1. Jochen Schiller “Mobile communications”, Pearson Education, New Delhi, Second Edition, 2004.
2. Theodore S Rappaport, “Wireless Communications Principles and Practice”, Pearson Education, New Delhi, Second Edition, 2003.
3. Siva Ram Murthy C and Manoj B S “Ad-hoc Wireless Networks, Architectures and Protocols” Pearson Education, New Delhi, 2005.
4. Charles E Perkins, “Mobile IP: Design Principles and Practice”, Addison Wesley, USA, 1999.

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3. www.powershow.com

PAE16352 SOFT COMPUTING 3 0 0 3

COURSE OBJECTIVES

- To study different types of optimization techniques
- To study genetic algorithms
- To gain knowledge in neural networks
- To study and analyze fuzzy logic
- To understand the Neuro fuzzy modeling

UNIT I EVOLUTION OF COMPUTING 9

Evolution of Computing - Soft Computing Constituents – From Conventional AI to Computational Intelligence - Machine Learning Basics

UNIT II GENETIC ALGORITHMS 9

Introduction, Building block hypothesis, working principle, Basic operators and Terminologies like individual, gene, encoding, fitness function and reproduction, Genetic modeling: Significance of Genetic operators, Inheritance operator, cross over, inversion & deletion, mutation operator, Bitwise operator, GA optimization problems, JSPP (Job Shop Scheduling Problem), TSP (Travelling Salesman Problem),Differences & similarities between GA & other traditional methods, Applications of GA.

UNIT III NEURAL NETWORKS 9

Machine Learning using Neural Network, Adaptive Networks – Feed Forward Networks– Supervised Learning Neural Networks – Radial Basis Function Networks - Reinforcement Learning– Unsupervised Learning Neural Networks – Adaptive Resonance Architectures – Advances in Neural Networks

UNIT IV FUZZY LOGIC AND SIMULATED ANNEALING 9

Fuzzy Sets – Operations on Fuzzy Sets – Fuzzy Relations – Membership Functions-Fuzzy Rules and Fuzzy Reasoning – Fuzzy Inference Systems – Fuzzy Expert Systems – Fuzzy Decision Making, Annealing, Boltzmann machine – learning – application – Counter Propagation Network – architecture – training - Applications

UNIT V ADVANCED NEURO-FUZZY MODELING 9

Adaptive Neuro-Fuzzy Inference Systems – Coactive Neuro-Fuzzy Modeling – Classification and Regression Trees – Data Clustering Algorithms – Rule base Structure Identification – Neuro-Fuzzy Control – Case Studies.

TOTAL: 45 PERIODS

COURSE OUTCOMES

At the end of this course, the students will be able to

- know the fundamentals of soft computing
- understand the genetic algorithm
- design the neural networks

- understand fuzzy logic
- perform advanced neuro-fuzzy modeling

REFERENCES

1. Jyh-Shing Roger Jang, Chuen-Tsai Sun, Eiji Mizutani, "Neuro-Fuzzy and Soft Computing", Prentice-Hall of India, 2003.
2. S.Rajasekaran and G.A.Vijayalakshmi Pai, **"**Neural networks, Fuzzy logics and Genetic algorithms"**,** Prentice Hall of India, 2003.
3. Kwang H.Lee, "First course on Fuzzy Theory and Applications", Springer–Verlag Berlin Heidelberg, 2005.
4. James A. Freeman and David M.Skapura, "Neural networks algorithms, applications, and programming techniques", Pearson edition, 2003.
5. David E.Goldberg, **"**Genetic Algorithms in Search, Optimization, and Machine Learning", Pearson Education, Asia, 2001**.**

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PAE16353 HIGH PERFORMANCE NETWORKS 3 0 0 3

COURSE OBJECTIVES

- To develop a comprehensive understanding of multimedia networking applications.
- To describe the types of VPN and tunneling protocols for security.
- To discriminate network security in many layers and network management.
- To classify various Network security and management.

UNIT I SWITCHING AND ROUTING 9

Review of OSI, TCP/IP; Multiplexing, Modes of Communication, Switching, Routing - SONET – DWDM – DSL – ISDN – BISDN, ATM, Architecture of 802.11

UNIT II MULTIMEDIA NETWORKING APPLICATIONS 9

Streaming stored Audio and Video – Best effort service – protocols for real time interactive applications – Beyond best effort – scheduling and policing mechanism – integrated services –RSVP- differentiated services.

UNIT III ADVANCED NETWORKS CONCEPTS 9

VPN-Remote-Access VPN, site-to-site VPN, Tunneling to PPP, Security in VPN.MPLS- operation, Routing, Tunneling and use of FEC, Traffic Engineering, MPLS based VPN, overlay networks- P2P connections.

UNIT IV CONGESTION AND TRAFFIC MODELING 9

Effects of congestion, Congestion control, Little's theorem, Need for modeling, Poisson modeling and its failure, Non- poisson models, ABR traffic management, GBR traffic Management, Network performance evaluation.

UNIT V NETWORK SECURITY AND MANAGEMENT 9

Principles of cryptography – Authentication – integrity – key distribution and certification – Access control and: fire walls – attacks and counter measures – security in many layers. Infrastructure for network management – The internet standard management framework – SMI, MIB, SNMP, Security and administration – ASN.1

TOTAL: 45 PERIODS

COURSE OUTCOMES

At the end of this course, the students will be able to

- gain a comprehensive knowledge in multimedia networking applications
- illustrate the types of VPN and tunneling protocols for security
- understand the various ways of controlling the traffic and its methods
- classify network security in many layers and network management

REFERENCES

1. J.F. Kurose & K.W. Ross, “Computer Networking- A top down approach featuring the internet”, Pearson, 2nd edition, 2003.
2. Aunuragkumar, D. M Anjunath, Joy kuri, “Communication Networking”, Morgan Kaufmann Publishers, 1ed 2004.
3. HersentGurle & petit, “IP Telephony, packet Pored Multimedia communication Systems”, Pearson education 2003.
4. Fred Halsall and Lingana Gouda Kulkarni, “Computer Networking and the Internet” fifth edition, Pearson education 2006
5. Nader F.Mir, “Computer and Communication Networks”, first edition, 2010

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3. www.freevideolectures.com

ELECTIVE IV

PAE16451 VLSI DESIGN TECHNIQUES 3 0 0 3

COURSE OBJECTIVES

- To study the basics of MOS transistor and IC fabrication.
- To learn inverters characteristics and logic function.
- To learn circuit characterization and performance estimation.
- To study VLSI circuits.
- To learn Verilog HDL and design VLSI circuits.

UNIT I VLSI DESIGN PROCESS AND MOS TRANSISTOR THEORY 9

VLSI Design Process – Architectural Design – Logical Design – Physical Design – Layout Styles –Full custom, Semicustom approaches.MOS transistors, CMOS logic, MOS transistor theory – Introduction, Enhancement mode transistor action, Ideal I-V characteristics, Simple MOS capacitance Models, Detailed MOS gate capacitance model, Detailed MOS Diffusion capacitance model, Non ideal I-V effects, DC transfer characteristics, VLSI Design flow.

UNIT II INVERTERS AND LOGIC GATES 9

NMOS and CMOS Inverters, Stick diagram, Inverter ratio, DC and transient characteristics , switching times, Super buffers, Driving large capacitance loads, CMOS logic structures , Transmission gates, Static CMOS design, dynamic CMOS design.

UNIT III CIRCUIT CHARACTERIZATION AND PERFORMANCE ESTIMATION 9

Resistance estimation, Capacitance estimation, Inductance, switching characteristics, transistor sizing, power dissipation and design margining, Charge sharing - Scaling

UNIT IV VLSI SYSTEM COMPONENTS CIRCUITS 9

Multiplexers, Decoders, comparators, priority encoders, Shift registers- Arithmetic circuits – Ripple carry adders, Carry look ahead adders, High-speed adders, Multipliers.

UNIT V VERILOG HARDWARE LANGUAGE 9

Overview of digital design with Verilog HDL, hierarchical modeling concepts, modules and port definitions, gate level modeling, data flow modeling, behavioral modeling, task & functions, Test Bench.

TOTAL: 45 PERIODS

COURSE OUTCOMES

At the end of this course, the students will be able to

- understand basics of MOS transistor and IC fabrication, inverters characteristics and logic function.
- estimate the circuit characterization and performance estimation.
- understand the concepts of VLSI circuits.
- understand verilog HDL and design VLSI circuits.

REFERENCES

1. Jan M Rabaey, " Digital Integrated Circuits", Prentice Hall of India, 2002
2. Sung-Mo Kang and Yusuf Leblebici, "CMOS Digital Integrated Circuits- Analysis and Design", Tata McGraw Hill, 2003.
3. SamirPalnitkar, "Verilog HDL", Pearson Education, 2nd Edition, 2004.
4. EugeneD.Fabricius, "Introduction to VLSI Design", McGraw Hill International Editions, 1990.
5. J.Bhasker, B.S.Publications, "A Verilog HDL Primer", 2nd Edition, 2001.

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1. www.nptel.ac.in/courses/117106093
2. www.nptel.ac.in/syllabus/syllabus.php?subjectId=117101004
3. www.buffalolib.org/vufind/Record/592861/Details

PAE16452 FIBER OPTIC SENSORS 3 0 0 3

COURSE OBJECTIVES

- To understand sensor technology and the basic concepts of grating sensor
- To know about distributed and magnetic sensors.
- To learn about the chemical and biosensors
- To study the applications of sensors

UNIT I SENSOR TECHNOLOGY 9

The Emergence of Fiber Optic Sensor Technology-Optical Fibers-Light Sources-Optical Detectors-Optical Modulators- Intensity modulated sensors, Microbendstrain intensity modulated sensor, Liquid level type hybrid sensor, internal effect intensity modulated sensor, Diffraction grating sensors and Interferometric sensors-Fabryperot, Mach Zender, Michelson and Sagnac sensors,

UNIT II GRATING SENSORS 9

Multimode Grating and Polarization Sensors-Sensors Based on Relative Movement of Opposed Gratings-Grating Period Modulation-Sensors Based on the Photo elastic Effect-Retardation Plates- Fiber Grating Sensors

UNIT III DISTRIBUTED AND MAGNETIC SENSORS 9

Fiber Optic distributed and Magnetic Sensor-Distributed Sensing- Basic Principles of Sensor Multiplexing- Interferometric Sensor Multiplexing- Faraday effect sensors- Magnetostrictive – Lorentz force sensors-Evanescent Field Absorption Sensors

UNIT IV CHEMICAL AND BIOSENSOR 9

Fiber Optic Chemical and Biosensor: Reagent Mediated sensor-Humidity sensor – pH sensor -Hydrogen sensor - CO2 sensor – Ammonia sensor - Chloride sensor – Glucose sensor – Oxygen sensor - Surface Plasmonic Resonance based sensor

UNIT V APPLICATIONS 9

Industrial Applications of Fiber Optic Sensors : Temperature – Pressure - fluid level – flow – position - vibration - rotation measurements - Current -voltage measurement - Chemical analysis. Introduction to smart structures - Applications –skins

TOTAL: 45 PERIODS

COURSE OUTCOMES

At the end of this course, the students will be able to

- know the sensor technology
- understand the sensor concepts of grating sensor
- know the sensor magnetic sensors.
- gain knowledge in the sensor and biosensor.
- study the applications of sensor.

REFERENCES

1. Eric Udd, William B. Spillman, Jr., “Fiber Optic Sensors: An Introduction for Engineers and Scientists”, John Wiley & Sons 2011.
2. Bhagavānadāsa Gupta, Banshi Das Gupta, “Fiber Optic Sensors: Principles and Applications”, New India Publishing 2006.
3. David A. Krohn, “Fiber optic sensors: fundamentals and applications”, ISA Publishing 2000
4. Francis T.S. Yu, Shizhuo Yin, Paul B. Ruffin, “Fiber Optic Sensors”, CRC Press Publisher, 2010.

WEB LINKS

1. www.iitg.ernet.in/physics/fac/skhijwania/pubInvited.html
2. www.freevideolectures.com
3. www.lightwaveonline.com

PAE16453 DIGITAL SIGNAL PROCESSING INTEGRATED CIRCUITS 3 0 0 3

COURSE OBJECTIVES

- To familiarize the number systems concept and arithmetic units
- To understand the concepts of digital signal processing.
- To study the concepts and gain knowledge about digital filters.
- To study DSP architectures.
- To understand the Design of DSP integrated circuit.

UNIT I NUMBER SYSTEMS AND ARITHMETIC UNITS 9

Conventional Number system - Redundant Number system - Residue Number System - Bit Parallel and Bit Serial Arithmetic - Distributed arithmetic - Basic Shift Accumulator - Reducing the memory size - Complex multipliers - improved shift-Accumulator

UNIT II DIGITAL SIGNAL PROCESSING 9

Digital signal processing, Sampling of analog signals - Selection of sample frequency - Signal-processing systems - Frequency response - Transfer functions - Signal flow graphs - Filter structures - Adaptive DSP algorithms - DFT-The Discrete Fourier Transform - FFT-The Fast Fourier Transform Algorithm, Image coding - Discrete cosine transforms.

UNIT III DIGITAL FILTERS AND FINITE WORD LENGTH EFFECTS 9

FIR filters - FIR filter structures - FIR chips - IIR filters - Specifications of IIR filters - Mapping of analog transfer functions - Mapping of analog filter structures - Multirate systems - Interpolation with an integer factor L - Sampling rate change with a ratio L/M - Multirate filters - Finite word length effects - Parasitic oscillations - Scaling of signal levels - Round-off noise- measuring round-off noise- Coefficient sensitivity- Sensitivity and noise

UNIT IV DSP INTEGRATED CIRCUITS AND VLSI CIRCUIT TECHNOLOGY 9

Standard digital signal processors - Application specific IC’s for DSP - DSP systems - DSP system design - Integrated Circuits design - MOS transistors - MOS Logic - VLSI Process technologies - Trends in CMOS technologies

UNIT V DSP ARCHITECTURES AND SYNTHESIS OF DSP ARCHITECTURES 9

DSP system architectures - Standard DSP architecture - Ideal DSP architectures - Multiprocessors and multi computers - Systolic and Wave front arrays - Shared memory architectures - Mapping of DSP algorithms onto hardware - Implementation based on complex PEs - Shared memory architecture with Bit – serial PEs.

TOTAL: 45 PERIODS

COURSE OUTCOMES

At the end of this course, the students will be able to

- understand the concepts of DSP
- design digital filters and understand the finite word length effects in the same
- understand DSP architectures.
- explain DSP integrated circuit and VLSI circuit technologies

REFERENCES

1. Lars Wanhammer, **"**DSP Integrated Circuits**"**, Academic press, New York 1999.
2. A.V.Oppenheim et.al, "Discrete-time Signal Processing", Pearson education, 2000.
3. Emmanuel C. Ifeachor, Barrie W. Jervis, **"**Digital signal processing A practical approach**",** Second edition, Pearson education, Asia 2001.
4. Keshab K.Parhi, "VLSI digital Signal Processing Systems design and Implementation", John Wiley& Sons, 1999.
5. Bayoumi & Magdy A., "VLSI Design Methodologies for Digital Signal Processing Architectures", BS Publications, 2005.

WEB LINKS

1. www.learnerstv.com/Free-engineering-video-lecture-courses.htm
2. www.nptelvideos.in/2012/11/digital-integrated-circuits.html
3. www.satishkashyap.com/p/video-lectures.html

PAE16454 RF SYSTEM DESIGN 3 0 0 3

COURSE OBJECTIVES

- To learn RF design and circuit board components
- To understand various impedance transformers and biasing networks
- To study the basic RF components
- To acquire knowledge about RF filters and RF synthesizer
- To study the basic RF mixers and oscillators

UNIT I CMOS PHYSICS, TRANSCEIVER SPECIFICATIONS AND ARCHITECTURES 9

CMOS: Introduction to MOSFET Physics – Noise: Thermal, shot, flicker, popcorn noise Transceiver Specifications: Two port Noise theory, Noise Figure, THD, IP2, IP3, Sensitivity, SFDR, Phase noise - Specification distribution over a communication link Transceiver Architectures: Receiver: Homodyne, Heterodyne, Image reject, Low IF Architectures – Transmitter: Direct up conversion, Two step up conversion.

UNIT II IMPEDANCE MATCHING AND AMPLIFIERS 9

S-parameters with Smith chart – Passive IC components - Impedance matching networks Amplifiers: Common Gate, Common Source Amplifiers – OC Time constants in bandwidth estimation and enhancement – High frequency amplifier design Low Noise Amplifiers: Power match and Noise match – Single ended and Differential LNAs – Terminated with Resistors and Source Degeneration LNAs.

UNIT III FEEDBACK SYSTEMS AND POWER AMPLIFIERS 9

Feedback Systems: Stability of feedback systems: Gain and phase margin, Root-locus techniques – Time and Frequency domain considerations – Compensation Power Amplifiers: General model – Class A, AB, B, C, D, E and F amplifiers – Linearization Techniques – Efficiency boosting techniques – ACPR metric – Design considerations.

UNIT IV PLL AND FREQUENCY SYNTHESIZERS 9

PLL: Linearised Model – Noise properties – Phase detectors – Loop filters and Charge pumps Frequency Synthesizers: Integer-N frequency synthesizers – Direct Digital Frequency synthesizers.

UNIT V MIXERS AND OSCILLATORS 9

Mixer: characteristics – Non-linear based mixers: Quadratic mixers – Multiplier based mixers: Single balanced and double balanced mixers – sub sampling mixers Oscillators: Describing Functions, Colpitt's oscillators – Resonators – Tuned Oscillators – Negative resistance oscillators – Phase noise.

TOTAL: 45 PERIODS

COURSE OUTCOMES

At the end of this course, the students will be able to

- understand various RF issues

- gain knowledge in the impedance transformation
- know about active RF component, matching and biasing networks
- understand the concepts of RF filter design and their implementation using software
- design the operation of RF oscillators and mixers and their design

REFERENCES

1. T.Lee, "Design of CMOS RF Integrated Circuits", Cambridge, 2004.
2. Reinhold Ludwig and Powel Bretchko, "RF Circuit Design – Theory and Applications", Pearson Education Asia, 2006.
3. Kai Chang, Inder Bahl and Vijay Nair, "RF and Microwave Circuit and Component Design for Wireless Systems", John Wiley and Sons, 2002.
4. Jan Crols, MichielSteyaert, "CMOS Wireless Transceiver Design", Kluwer Academic Publishers, 1997
5. B.Razavi, "Design of Analog CMOS Integrated Circuits", McGraw Hill, 2001.

WEB LINKS

1. www.nptel.ac.in/courses/117102012
2. www.ee.sharif.edu/~mmic/links.html
3. www.freevideolectures.com

PAE16455 SOLID STATE DEVICE MODELING AND SIMULATION 3 0 0 3

COURSE OBJECTIVES

- To understand the basic semiconductor physics.
- To understand basic concepts bipolar device modeling.
- To understand the operation of MOSFET modeling.
- To study the parameter measurement and optoelectronic device modeling.
- To acquire knowledge about optoelectronic device modeling.

UNIT I BASIC SEMICONDUCTOR PHYSICS 9

Quantum Mechanical Concepts, Carrier Concentration, Transport Equation, Band gap, Mobility and Resistivity, Carrier Generation and Recombination, Avalanche Process, Noise Sources - Diodes : Forward and Reverse biased junctions – Reverse bias breakdown – Transient and AC conditions –- Static and Dynamic behavior- Small and Large signal models – SPICE model for a Diode – Temperature and Area effects on Diode Model Parameters.

UNIT II BIPOLAR DEVICE MODELING 9

Transistor Models: BJT – Transistor Action – Minority carrier distribution and Terminal currents - Switching- Eber - Molls and Gummel Poon Model, SPICE modeling - temperature and area effects.

UNIT III MOSFET MODELING 9

OS Transistor – NMOS, PMOS – MOS Device equations - Threshold Voltage – Second order effects - Temperature Short Channel and Narrow Width Effect, Models for Enhancement, Depletion Type MOSFET, CMOS Models in SPICE.

UNIT IV PARAMETER MEASUREMENT 9

Bipolar Junction Transistor Parameter – Static Parameter Measurement Techniques – Large signal parameter Measurement Techniques, Gunmel Plots, MOSFET: Long and Short Channel Parameters, Measurement of Capacitance.

UNIT V OPTOELECTRONIC DEVICE MODELING 9

Static and Dynamic Models, Rate Equations, Numerical Technique, Equivalent Circuits, Modeling of LEDs, Laser Diode and Photo detectors.

TOTAL: 45 PERIODS

COURSE OUTCOMES

At the end of this course, the students will be able to

- know the fundamental of physics and BJT modeling
- understand MOSFET modeling and optoelectronic device modeling
- measure parameter measurement

REFERENCES

1. Ben.G..Streetman, “Solid State Devices”, Prentice Hall, 1997.
2. Giuseppe Massobrio and Paolo Antogentti, “Semiconductor Device Modeling with SPICE” Second Edition, McGraw-Hill Inc, New York, 1993.
3. Tyagi M.S. “Introduction to Semiconductor Devices”, 2nd Edition Mc Graw Hill, New York, 1981.
4. S.M.Sze “Semiconductor Devices - Physics and Technology”, John Wiley and sons, 1985.
5. Mohammed Ismail & Terri Fiez “Analog VLSI-Signal & Information Processing” 1stED, Tata McGraw Hill Publishing company Ltd 2001.

WEB LINKS

1. www.nptel.ac.in/video.php?subjectId=117106091
2. www.freevideolectures.com
3. www.satishkashyap.com/.../video-lectures-on-semiconductor-device.html