PAAVAI ENGINEERING COLLEGE, NAMAKKAL – 637 018

(AUTONOMOUS)

M.E. VLSI DESIGN

REGULATION 2016

(CHOICE BASED CREDIT SYSTEM)

CURRICULUM

SEMESTER III

Course Code	Course Title	L	T	P	C
PVL16301	Testing of VLSI Circuits	3	2	0	4
PVL1655*	Elective V	3	0	0	3
PVL1665*	Elective VI	3	0	0	3
PVL16302	Project Work (Phase I)	0	0	12	6

SEMESTER IV

Course Code	Course Title	L	T	P	C
PVL16401	Project Work (Phase II)	0	0	24	12

LIST OF ELECTIVES

ELECTIVE V

Course Code	Course Title	L	T	P	C
PVL16551	DSP Processor Architecture and Programming	3	0	0	3
PVL16552	Data Converters	3	0	0	3
PVL16553	Embedded Systems	3	0	0	3
PVL16554	Analysis and Design of Digital Integrated Circuits	3	0	0	3

ELECTIVE VI

Course Code	Course Title	L	T	P	C
PVL16651	Computer Architecture and Parallel Processing	3	0	0	3
PVL16652	RF IC Design	3	0	0	3
PVL16653	RF MEMS	3	0	0	3
PVL16654	Reconfigurable Computing	3	0	0	3

SEMESTER III

PVL16301 **TESTING OF VLSI CIRCUITS** **3 2 0 4**

COURSE OBJECTIVES

- To gain knowledge about digital testing as applied to VLSI design.
- To acquire knowledge of testing of algorithms for digital circuits
- To learn various testing methods for digital circuits.
- To learn memory testing.
- To gain knowledge about different levels of diagnosis.

UNIT I BASICS OF TESTING AND FAULT MODELING 15

Introduction to Testing - Faults in digital circuits - Modeling of faults - Logical Fault Models - Fault detection - Fault location - Fault dominance - Logic Simulation - Types of simulation - Delay models –Gate level Event-driven simulation.

UNIT II TEST GENERATION FOR COMBINATIONAL AND SEQUENTIAL CIRCUITS 15

Test generation for combinational logic circuits - Testable combinational logic circuit design - Test generation for sequential circuits - design of testable sequential circuits.

UNIT III DESIGN FOR TESTABILITY 15

Design for Testability - Ad-hoc design - Generic scan based design - Classical scan based design - System level DFT approaches.

UNIT IV BIST MEMORY TESTING 15

Built-In Self-Test - Test pattern generation for BIST - Circular BIST - BIST Architectures - Testable Memory Design - Test algorithms.

UNIT V LOGIC LEVEL AND SYSTEM LEVEL DIAGNOSIS 15

Logic Level Diagnosis - Diagnosis by UUT reduction - Fault Diagnosis for Combinational Circuits - Self-checking design - System Level Diagnosis.

TOTAL PERIODS 75

COURSE OUTCOMES

At the end of this course, students will be able to

- examine the basics of testing and fault modeling.
- examine different testing algorithms.
- analyze design for testability.
- syntheses the concepts of BIST and memory testing.
- evaluatethe different levels of fault diagnosis.

REFERENCES

1. M. Abramovici, M.A. Breuer and A.D. Friedman, “Digital Systems a Testable Design", Jaico Publishing House, 2002.
2. P.K. Lala, “Digital Circuit Testing and Testability”, Academic Press, 2002.
3. M.L. Bushnell and V.D. Agrawal, “Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits”, Kluwar Academic Publishers, 2002.

4. A.L. Crouch, “Design for Test for Digital IC's and Embedded Core Systems”, Prentice Hall International, 2002.

WEB LINKS

1. www.ee.ncu.edu.tw/~jfli/vlsi21/lecture/ch06.pdf
2. https://www.ece.cmu.edu/~ece322/LECTURES/Lecture25/Lecture25.pdf
3. nptel.ac.in/courses/106103116/
4. https://www.youtube.com/watch?v=Abld-fSxjNM
5. https://www.ee.iitb.ac.in/~viren/Courses/2014/EE709.htm

ELECTIVE V

PVL16551 DSP PROCESSOR ARCHITECTURE AND PROGRAMMING 3 0 0 3

COURSE OBJECTIVES

- To study the fundamentals of programmable DSPs.
- To study the architecture and various addressing modes of processor.
- To impart knowledge about the operation of ADSP and Analog processors.
- To study the architecture of advanced processors.
- To study the various addressing modes of TMS320C54X and TMS320C6Xprocessor

UNIT I FUNDAMENTALS OF PROGRAMMABLE DSPS 9

Multiplier and Multiplier accumulator (MAC) – Modified Bus Structures and Memory access in Programmable DSPs – Multiple access memory – Multi-port memory – VLIW architecture- Pipelining – Special Addressing modes in P-DSPs – On chip Peripherals.

UNIT II TMS320C3X PROCESSOR 9

Architecture – Data formats - Addressing modes – Groups of addressing modes- Instruction sets - Operation – Block Diagram of DSP starter kit – Application Programs for processing real time signals – Generating and finding the sum of series, Convolution of two sequences, Filter design

UNIT III ADSP PROCESSORS 9

Architecture of ADSP-21XX and ADSP-210XX series of DSP processors - Addressing modes –and assembly language instructions – Application programs –Filter design, FFT calculation

UNIT IV ADVANCED PROCESSORS I 9

Architecture of TMS320C54X: Pipe line operation, Addressing modes and assembly language instructions Introduction to Code Composer studio

UNIT V ADVANCED PROCESSORS II 9

Architecture of TMS320C6X - Architecture of Motorola DSP563XX – Comparison of the features of DSP family processors.

TOTAL PERIODS 45

COURSE OUTCOMES

At the end of this course, students will be able to

- analyze the procedure for various DSP system architecture
- diagnose the design methodologies in hardware and software.
- perform the identification of new developments in DSP systems.
- design and implement various signal processing techniques using DSP processors.
- examine the processors architecture and instructions.

REFERENCES

1. B.Venkataramani and M.Bhaskar, “Digital Signal Processors – Architecture, Programming and Applications”, Tata McGraw Hill Publishing Company Limited. New Delhi, 2003.
2. Yu Hen Hu, “Programmable digital signal processors: Architecture, Programming and application”, CRC press, 2001

3. Steven smith, “The scientist and engineers guide to digital signal processing”.
4. User guide, Texas Instrumentation, Analog Devices, Motorola.

WEB LINKS

1. www.elin.ttu.ee/~olev/lect1.pdf
2. https://www.youtube.com/watch?v=SKuywStjBLY
3. bwrcs.eecs.berkeley.edu/Classes/CS252/Notes/Lec10a-DSP1.pdf
4. nptel.ac.in/courses/108102045/9
5. www.ti.com/lit/pdf/spru194

PVL16552 **DATA CONVERTERS** **3 0 0 3**

COURSE OBJECTIVES

- To understand the basic concepts of data converters performances
- To know the A/D converters
- To know the hardware design techniques
- To study the concepts of digital correction and calibration
- To focus on the application of converters

UNIT I DATA CONVERSION FUNDAMENTAL, DATA CONVERTER PERFORMANCES 9

Sampling of Analog Signals - Quantization Error and Quantization Noise -Nyquist Rate and Oversampling – Conversion - Resolution and SNR- Reconstruction-Static Performances -Dynamic Performances – Distortion

UNIT II SAMPLE & HOLD CIRCUITS, LOW SPEED NYQUIST-RATE A/D CONVERTERS 9

Sampling switches, Conventional open loop and closed loop sample and hold architecture, Open loop architecture with miller compensation, multiplexed input architectures, recycling architecture switched capacitor architecture. CMOS Track and Sample and Hold-Diode Bridge T&H-Switched Emitter T&H-Accuracy and Speed-Integrating Converter-Successive Approximation Converters-Algorithmic A/D Converters.

UNIT III HIGH SPEED NYQUIST-RATE A/D CONVERTERS, OVERSAMPLING A/D CONVERTERS 9

Flash Converters-Two-Step Converters-Folding Converters-Interpolating Technique-Interleaved Converters-Pipeline Converters-Noise Shaping-First-Order Sigma-Delta - Second-Order Sigma-Delta -High-Order Sigma-Delta-Multi-bit Oversampling Converters-Practical Limit-Design Considerations

UNIT IV DIGITAL CORRECTION AND CALIBRATION, NYQUIST-RATE DACS 9

Digital - Correction-Linearization of Transfer Characteristics - Basic considerations – Switched Capacitor MDAC - Resistive based Architectures - Current Steering D/A Converters.

UNIT V PRECISION TECHNIQUES 9

Comparator offset cancellation - Op Amp offset cancellation - Calibration techniques - range overlap and digital correction.

TOTAL PERIODS 45

COURSE OUTCOMES

At the end of this course, students will be able to

- examine the fundamentals of data converters
- analyze the sample and hold circuit.
- perform A/D and D/A converters
- analyze about Data converters application

REFERENCES

1. D.A. Johns and K. Martin, “Analog Integrated Circuits and Systems”, McGraw-Hill, NY 1994
2. Rudy J, Van de Plassche, “CMOS Integrated Analog-to-Digital and Digital-to-Analog Converters”, BS Publications, 2005.
3. B. Razavi, “Principles of Data Conversion System Design”, The IEEE Press, New York, 1995.
4. Walt Kester Editor, “Analog-Digital Conversion”, analog devices, 2004

5. Franco Maloberti, “Data Converters”, Springer, 2007.

WEB LINKS

6. http://nptel.ac.in/courses/117106034/
7. www.nptel.ac.in/courses/108105057/Pdf/Lesson-18.pdf
8. nptel.ac.in/courses/106108100/pdf/Teacher_Slides/mod3/M3L8.pdf
9. https://www.youtube.com/watch?v=ZcTTkCWnQNg

PVL16553 **EMBEDDED SYSTEMS** **3 0 0 3**

COURSE OBJECTIVES

- To study the overview of architecture of embedded system
- To focus on processors used in embedded systems
- To study the various networks of embedded system
- To understand about real time systems and system design methodologies.
- To study the overview of architecture of embedded system

UNIT I EMBEDDED ARCHITECTURE **9**

Embedded Computers, Characteristics of Embedded Computing Applications, Challenges in Embedded System Design, Embedded System Design Process - Requirements, Specification, Architectural Design, Designing Hardware and Software Components, System Integration.

UNIT II EMBEDDED PROCESSOR AND COMPUTING PLATFORM **9**

ARM processor- Processor and memory organization, Data operations, Flow of control, SHARC processor-Memory organization, Data operations, Flow of control, Parallelism with instructions, CPU Bus configuration, ARM Bus, SHARC Bus, Memory Devices, Input and Output Devices. Design Example: Alarm Clock

UNIT III NETWORKS **9**

Distributed Embedded Architecture - Hardware and Software Architectures, Networks for embedded systems- I2C, CAN Bus, SHARC link ports, Ethernet, Myrinet, Internet. Network based design, Design Example: Elevator Controller.

UNIT IV REAL-TIME CHARACTERISTICS **9**

Clock driven Approach, Weighted round robin Approach, Priority driven Approach, Dynamic Versus Static systems, effective release times and deadlines, Optimality of the Earliest deadline first (EDF) algorithm, Off-line Versus On-line scheduling.

UNIT V SYSTEM DESIGN TECHNIQUES **9**

Design Methodologies, Requirement Analysis, Specification, System Analysis and Architecture Design, Quality Assurance, Design Example: Telephone PBX-Ink jet printer- Personal Digital Assistants, Set-top Boxes.

TOTAL PERIODS 45

COURSE OUTCOMES

At the end of this course, students will be able to

- examine the architecture of embedded system
- design embedded processor architecture.
- compare various networks of embedded system
- analyze real time systems
- demonstrate the basic difference between RTES and RTOS in system design

REFERENCES

1. Wayne Wolf, “Computers as Components: Principles of Embedded Computing System Design”, Morgan Kaufman Publishers, 2001.
2. Jane.W.S. Liu, “Real-Time systems”, Pearson Education Asia, 2000

3. C. M. Krishna and K. G. Shin , “Real-Time Systems”, McGraw-Hill, 1997
4. Frank Vahid and Tony Givargi, “Embedded System Design: A Unified Hardware/Software Introduction”, John Wiley & Sons, 2000.
5. Rajkamal, “Embedded Systems Architecture, Programming and Design”, TMH, First reprint, 2003

WEB LINKS

1. http://nptel.ac.in/video.php?subjectId=108102045
2. http://www.nptelvideos.in/2012/11/embedded-systems.html
3. http://nptel.ac.in/courses/108102045/18
4. nptel.ac.in/courses/106105036/

PVL16554 ANALYSIS AND DESIGN OF DIGITAL INTEGRATED CIRCUITS 3 0 0 3

COURSE OBJECTIVES

- To understand the MOS transistor circuit and its enhancement process.
- To acquire knowledge about generation of MOS inverter circuit for combinational and sequential circuits.
- To understand the concepts behind the high speed logic design.
- To study the concept of semiconductor memory design.
- To learn about Power distribution design-clocking and timing issues.

UNIT I DEEP SUBMICRON DIGITAL IC DESIGN, TRANSISTORS AND DEVICES-MOS AND BIPOLAR, FABRICATION, LAYOUT AND SIMULATION 9

Review of Digital Logic Gate Design-digital IC design-computer Aided Design of digital circuits-The MOS Transistor-Bipolar Transistor and circuits-IC Fabrication technology-Layout basics-modeling the MOS transistor for circuit simulation-SPICE MOS level1 device model-BSIM3 model-additional effects in MOS transistors-SOI technology.

UNIT II MOS INVERTERS CIRCUITS, STATIC MOS GATE CIRCUITS 9

Voltage transfer characteristics-noise margin definitions-resistive load inverter design-NMOS transistors as load devices-CMOS inverter-pseudo-NMOS inverters-sizing inverters- tristate inverters-CMOS gate circuits-complex CMOS gates-XOR and XNOR gates-multiplexer circuits – Flip-flops and latches – D flip-flops and latches – power dissipation in CMOS gates-power and delay trade-offs

UNIT III HIGH SPEED CMOS LOGIC DESIGN, TRANSFER GATE AND DYNAMIC LOGIC DESIGN 9

Switching time analysis – detailed load capacitance calculation – improving delay calculation with input slope - gate sizing for optimal path delay – optimizing path with logical effort – basic concepts of transfer gate – CMOS transmission gate logic – dynamic D latches and D flip-flops – domino logic –voltage bootstrapping

UNIT IV SEMICONDUCTOR MEMORY DESIGN, ADDITIONAL TOPICS IN MEMORY DESIGN, INTERCONNECT DESIGN 9

Introduction-MOS decoders – static RAM cell design - SRAM column I/O circuitry – memory architecture - content addressable memories - FPGA-dynamic Read - Write memories - Read Only memories-EPROMs and E^2PROMs - flash memory – FRAMs - interconnect RC delays - buffer insertion for very long wires - interconnect coupling capacitance - interconnect inductance - antenna effects.

UNIT V POWER GRID AND CLOCK DESIGN, LOW POWER CMOS LOGIC CIRCUITS, HIP INPUT AND OUTPUT CIRCUITS, DESIGN FOR TESTABILITY 9

Power distribution design-clocking and timing issues, phase-locked loops/delay-locked loops – low power design through voltage scaling – estimation and optimization of switching activity – reduction of switched capacitance – adiabatic logic circuits – ESD protection – input circuits – output circuits and L(di/dt) noise – on-chip clock generation and distribution – latch-ups and its prevention – fault types and models – controllability and observability – adhoc testable design techniques – scan based techniques – Built-In-Self Test(BIST) techniques – current monitoring I_{DDQ} test.

TOTAL PERIODS 45

COURSE OUTCOMES

At the end of this course, students will be able to

- evaluate the importance of logical design VLSI circuits.

- model different faults and carry out fault simulation in digital circuits.
- design high speed CMOS circuit.
- design memory device.
- analyze the testing process

REFERENCES

1. David A Hodges, Horace G Jackson, Resve A Saleh, "Analysis and design of Digital Integrated Circuits – in deep submicron technology", Tata McGraw Hill, Edition 2005.
2. Sung-Mo Kang, Yusuf Leblebici, "CMOS Digital Integrated Circuits-analysis and design", Tata McGraw Hill, Third edition-2003

WEB LINKS

1. ocw.mit.edu › Courses › Electrical Engineering and Computer Science
2. https://www.youtube.com/watch?v=2aRwFWhLk0o
3. ceit.aut.ac.ir/~shiry/lecture/Digital%20Electronics/084931951X.pdf
4. www.cse.wustl.edu/~vgruev/cse/463/

ELECTIVE VI

PVL16651 COMPUTER ARCHITECTURE AND PARALLEL PROCESSING 3 0 0 3

COURSE OBJECTIVES

- To study the fundamentals of parallel processing.
- To study the architecture of processor and memory organization.
- To impart knowledge about the operation of pipeline architecture.
- To study the architecture of vector processing and multithreading

UNIT I PRINCIPLES OF PARALLEL PROCESSING 9

Multiprocessors and Multicomputers – Multivector and SIMD Computers- PRAM and VLSI Models-Conditions of Parallelism- Program Partitioning and scheduling-program flow mechanisms- parallel processing applications- speed up performance law.

UNIT II PROCESSOR AND MEMORY ORGANIZATION 9

Advanced processor technology – superscalar and vector processors- memory hierarchy technology-virtual memory technology- Cache memory organization- Shared memory organization.

UNIT III PIPELINE AND PARALLEL ARCHITECTURE 9

Linear pipeline processors- Non linear pipeline processors- Instruction pipeline design- Arithmetic design-Superscalar and super pipeline design- Multiprocessor system interconnects- Message passing mechanisms.

UNIT IV VECTOR, MULTITHREAD AND DATAFLOW ARCHITECTURE 9

Vector Processing principle- Multivector Multiprocessors- Compound Vector processing- Principles of multithreading-fine grain multicomputers- scalable and multithread architectures – Dataflow and hybrid architectures.

UNIT V SOFTWARE AND PARALLEL PROCESSING 9

Parallel programming models- parallel languages and compilers- parallel programming environments-synchronization and multiprocessing modes- message passing program development- mapping programs onto multicomputers-multiprocessor UNIX design goals- MACH/OS kernel architecture- OSF/1 architecture and applications.

TOTAL PERIODS 45

COURSE OUTCOMES

At the end of this course, students will be able to

- analyze the procedure for various DSP System Architecture
- diagnose the design methodologies in hardware and software.
- perform identification of new developments in DSP systems
- design and implement various signal processing techniques using DSP processors.

REFERENCES

1. Kai Hwang, “Advanced Computer Architecture”, TMH 2001.
2. William Stallings, “Computer Organization and Architecture”, McMillan Publishing Company,1990
3. M.J. Quinn, “Designing efficient Algorithms for parallel computer”, McGraw Hill International,1994

WEB LINKS

1. http://nptel.ac.in/courses/106102114/
2. http://nptel.ac.in/courses/106106092/
3. http://iitvideos.blog.com/

PVL16652 **RF IC DESIGN** **3 0 0 3**

COURSE OBJECTIVES

- To understand the basics of RFICs.
- To understand the RF components and modeling.
- To study the basics of impedance matching in RFICs
- To learn the design of active circuits in RFICs
- To understand the RF Oscillators and mixers.

UNIT I INTRODUCTION **9**

Importance of RF design, dimensions and units, RF Behavior of passive components, chip components and circuit board considerations, RF circuit manufacturing processes , introduction to random process and noises, review of thermal noise, noise models and circuit noise calculations

UNIT II ACTIVE RF COMPONENTS AND MODELING **9**

Semiconductor basics, RF Diode, bi-polar Junction Transistor, RF Field Effect Transistors, Metal Oxide Semiconductor Transistors, High electron mobility transistors, diode and transistor models, Measurement of active devices.

UNIT III MATCHING-BIASING NETWORK AND RF TRANSISTOR AMPLIFIER DESIGN **9**

Impedance Matching using Discrete Components, Micro-strip line Matching Networks, Amplifier classes of operations and biasing networks, Amplifier power relations, Stability considerations, Constant gain, Noise Figure circles, constant VSWR Circles, Broad band High power and multistage amplifiers.

UNIT IV MODULATORS AND DEMODULATORS TECHNIQUES, RF TRANSCEIVERS ARCHITECTURES **9**

Modulators and demodulators, their structures and electrical schemes, transceivers and architectures, Transceivers functions and their characteristics, direct conversions and super heterodyne receivers.

UNIT V RF OSCILLATORS, MIXERS AND PHASE LOCKED LOOPS (PLL) **9**

Basic Oscillator models, High-Frequency Oscillator Configuration, Basic characteristics of Mixers-Single ended, double ended, integrated active, and image reject mixers, Phase locked loops and frequency synthesis, Basic building block of the PLL, PLL synthesizers for radio applications.

TOTAL PERIODS 45

COURSE OUTCOMES

At the end of this course, students will be able to

- evaluate of application of RFICs.
- compare various technologies and parameters.
- examine impedance matching and their design and simulation using software
- syntheses applications of passive circuits and active circuits in RFICs.

REFERENCES

1. Reinhold Ludwig and Gene Bogdanov, “RF Circuit Design”, second edition, Pearson Education, 2009.
2. D. M. Pozar, “Microwave engineering”, second edition, N.Y., John Wiley and Sons, 1998.

3. B.P.Lathi, “Modern digital and analog communication systems”, third edition, N.Y., Oxford University press, 1998.
4. B.Sklar, “Digital communications-fundamentals and applications”, second edition, Prentice Hall PTR,New Jersey, 2001.

WEB LINKS

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2. rfic.eecs.berkeley.edu/~niknejad/ee242/lectures.html
3. www.ee.iitm.ac.in/~ani/2011/ee6240/lectures.html
4. whites.sdsmt.edu/classes/ee322/class_notes/322Lecture22.pdf

PVL16653 **RF MEMS** **3 0 0 3**

COURSE OBJECTIVES

- To understand the basic concepts of RF MEMS
- To acquire the basic knowledge of Micro machined Components I
- To know about the micro machined components II
- To understand the key concepts of beam structures and micro strip antennas
- To know the design analysis using RF MEMS

UNIT I INTRODUCTION AND SWITCHING 9

Overview of RF MEMS, Road map, fabrication process design and testing, Applications, RF MEMS relays and switches: Switch parameters, Actuation mechanisms, Bistable relays and micro actuators, Dynamics of switching operation.

UNIT II MICRO MACHINED INDUCTORS AND CAPACITORS 9

MEMS inductors and capacitors: Micro machined inductor, Effect of inductor layout, Modeling and design issues of planar inductor, Gap tuning and area tuning capacitors, Dielectric tunable capacitors.

UNIT III RF MEMS PHASE SHIFTERS 9

MEMS phase shifters: Types. Limitations - Switched delay lines, Micro machined transmission lines, coplanar lines, Micro machined directional coupler and mixer.

UNIT IV MICRO MACHINED FILTERS &ANTENNAS 9

Micro machined RF filters: Modeling of mechanical filters, Electrostatic comb drive, Micromechanical filters using comb drives, Electrostatic coupled beam structures. Micro machined antennas: Micro strip antennas – design parameters, Micromachining to improve performance, Reconfigurable antennas.

UNIT V RF MEMS DESIGN ANALYSIS 9

MEMS Physical Modeling, Physical and practical aspects of RF circuit design: X –Band RF MEMS Phase shifter for radar system applications, FBAR filter for PCS applications, A Ka-Band millimeter-wave tunable filter. Impedance mismatch effects in RF MEMS, RF/Microwave substrate properties, MEMS-Resonators.

TOTAL PERIODS 45

COURSE OUTCOMES

At the end of this course, students will be able to

- examine basic knowledge of RF MEMS and Switching
- evaluate tuning elements
- demonstrate critical thinking and problem solving capabilities
- identify the major RF filters and antennas.
- design and analyze circuits using RF MEMS

REFERENCES

1. V.K.Varadan, KJ.Vinoy,K.N.Jose, “RFMEMS and their Applications”, Wiley, 2003.
2. H.J.Delos Santos, “RF MEMS circuit Design for Wireless Communications”, Artech House, 2002.
3. Gabriel.M.Rebeiz, “RF MEMS Theory, Design and Technology”, John Wiley, 2003

WEB LINKS

1. www.memtronics.com/page.aspx?page-id=13
2. http://iitvideos.blog.com/
3. ocw.mit.edu › Courses › Electrical Engineering and Computer Science

PVL16654 RECONFIGURABLE COMPUTING 3 0 0 3

COURSE OBJECTIVES

- To familiarize themselves with the PLD devices.
- To understand the concepts of reconfigurable architectures.
- To study the concepts and gain knowledge about operating systems.
- To study mapping and placement.
- To understand the application of FPGA.

UNIT I DEVICE ARCHITECTURE 9

General Purpose Computing Vs Reconfigurable Computing – Simple Programmable Logic Devices – Complex Programmable Logic Devices – FPGAs – Device Architecture - Case Studies.

UNIT II RECONFIGURABLE COMPUTING ARCHITECTURES AND SYSTEMS 9

Reconfigurable processing fabric architectures – RPF integration into traditional computing systems – reconfigurable computing systems – case studies – reconfiguration management.

UNIT III PROGRAMMING RECONFIGURABLE SYSTEMS 9

Compute Models - Programming FPGA Applications in HDL – Compiling C for Spatial Computing – operating System Support for Reconfigurable Computing.

UNIT IV MAPPING DESIGNS TO RECONFIGURABLE PLATFORMS 9

The Design Flow - Technology Mapping – FPGA Placement and Routing – Configuration Bit stream Generation – Case Studies with Appropriate Tools.

UNIT V APPLICATION DEVELOPMENT WITH FPGAS 9

Case Studies of FPGA Applications – System on a programmable Chip (SoPC) Designs

TOTAL PERIODS 45

COURSE OUTCOMES

At the end of this course, students will be able to

- examine PLD devices.
- analyze the concepts of reconfigurable architectures.
- compare operating systems.
- examine mapping and placement.
- design the application of FPGA.

REFERENCES

1. Maya B. Gokhale and Paul S. Graham, “Reconfigurable Computing: Accelerating Computation with Field-Programmable Gate Arrays”, Springer, 2005.
2. Scott Hauck and Andre Dehon (Eds.), “Reconfigurable Computing – The Theory and Practice of FPGA-Based Computation”, Elsevier / Morgan Kaufmann, 2008.
3. Christophe Bobda, “Introduction to Reconfigurable Computing – Architectures, Algorithms and Applications”, Springer, 2010.

WEB LINKS

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3. www.ee.ryerson.ca/~lkirisch/ee8603/.../EE8603_Course_Outline.pdf
4. www.ecs.umass.edu/ece/tessier/courses/636/